formation of the passivation film 716 without exposing the device to the air. The successive processing for avoiding exposure to the air may further be extended to include the step of bonding the cover member 718.

The TFTs in this embodiment are each characterized in that: a gate electrode is formed from a conductive film having two layers; almost no difference in concentration is found between low concentration impurity regions that are formed between a channel formation region and a drain region, thereby forming a gentle concentration gradient; and the low concentration impurity regions are classified into one that overlaps with the underlying gate electrode (this one is called a GOLD region) and one that does not overlap the gate electrode (this one is called an LDD region). The edges of a gate insulating film, namely, a region above the region that does not overlap the gate electrode and above a high concentration impurity region are tapered.

In the light emitting device of this embodiment, if there is a pin hole in the light emitting layer 713b, it causes a defect portion where the hole injection layer 713a and the cathode 714 are brought into contact through the pin hole. The defect portion can be changed into a transmuted portion 715 by the repairing method of the present invention, resulting in a raise in resistance. Therefore the other part of the pixel than the pin hole can have increased luminance and degradation of a part of the EL layer that surrounds the pin hole is not accelerated.

This embodiment shows the structure of the pixel portion and of the driving circuit only. However, the manufacturing process according to this embodiment can also form logic circuits such as a signal divider circuit, a D/A converter, an operation amplifier, and a γ correction circuit on the same insulator which holds the pixel portion and the driving circuit. Additionally, a memory and a microprocessor may be formed.

The structure of this embodiment can be combined with any of Embodiments 1, 2, 3, 4, 6, and 8.

[Embodiment 10]

This embodiment gives descriptions on a sectional view of a light emitting device to which a repairing method of the present invention is applied.

In Fig. 17, a p-channel TFT 200 and an n-channel TFT 201 of a driving circuit are formed on the same substrate on which an EL driving TFT 203, a switching TFT 204, and a capacitor storage 205 are formed to constitute a pixel portion.

The p-channel TFT 200 of the driving circuit is comprised of: a conductive layer 220 having a second taper shape and functioning as a gate electrode; a channel formation region 206; a third impurity region 207a to function as a source region or a drain region; a fourth impurity region (A) 207b serving as an LDD region that does not overlap the gate electrode 220; and a fourth impurity region (B) 207c serving as an LDD region that partially overlaps the gate electrode 220.

The n-channel TFT 201 of the driving circuit is comprised of: a conductive layer 221 having a second taper shape and functioning as a gate electrode; a channel formation region 208; a first impurity region 209a to function as a source region or a drain region; a second impurity region (A) 209b serving as an LDD region that does not overlap the gate electrode 221; and a second impurity region (B) 209c serving as an LDD region that partially overlaps the gate electrode 221. While the channel length is 2 to 7 μm, the length of a portion where the second impurity region (B) 209c overlaps the gate electrode 221 is set to 0.1 to 0.3 μm. The length of this L_{OV} region is controlled by adjusting the thickness of the gate electrode 221 and the angle of the tapered portion. With this LDD region formed in the n-channel TFT, the high electric field generated in the vicinity of the

drain region is eased to prevent creation of hot carriers and thus prevent degradation of the TFT.

Similarly, the EL driving TFT 203 is comprised of: a conductive layer 223 having a second taper shape and functioning as a gate electrode; a channel formation region 212; a third impurity region 213a to function as a source region or a drain region; a fourth impurity region (A) 213b serving as an LDD region that does not overlap the gate electrode 223; and a fourth impurity region (B) 213c serving as an LDD region that partially overlaps the gate electrode 223.

Logic circuits such as a shift register circuit and a buffer circuit, and a sampling circuit having an analog switch constitute the driving circuit. In Fig. 17, the TFTs of these circuits have a single gate structure in which one gate electrode is placed between a source and a drain that form a pair. However, the TFTs may have a multi-gate structure in which a plurality of electrodes are placed between the source and the drain that form a pair.

The drain region of the EL driving TFT 203 is connected to a pixel electrode 271 through a wiring line 231. An EL layer 272 is formed from a known organic EL material so as to contact with the pixel electrode 271. A cathode 273 is formed so as to contact with the EL layer 272.

The switching TFT 204 is comprised of: a conductive layer 224 having a second taper shape and functioning as a gate electrode; channel formation regions 214a and 214b; first impurity regions 215a and 217 to function as source regions or drain regions; a second impurity region (A) 215b serving as an LDD region that does not overlap the gate electrode 224; and a second impurity region (B) 215c serving as an LDD region that partially overlaps the gate electrode 224. The length of a portion where the second impurity region (B) 215c overlaps the gate electrode 224 is set to 0.1 to 0.3 μm. The